APPLICATION NOTE:

Application of the TDA9177: YUV-Transient Improvement - Processor (LTP-Booster)

AN96049

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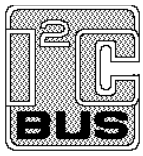
Abstract

This note gives a description of the Transient Improvement-processor(LTP-Booster)



Purchase of Philips I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips. This specification can be ordered using the code 9398 393 40011.

TDA9177 Application note: LTP-BOOSTER Description

Author(s):

G.C.M.Rossen
Design & Application, consumer IC's Nijmegen,
The Netherlands

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Summary

The TDA9177 (nickname = LTP-BOOSTER) is an I^2C-bus controlled sharpness improvement IC with additional inputs for 6-bit AD conversion to facilitate additional parameter measurement (e.g. ambient light control).
It should preferably be used in front of a RGB-processor with YUV-interface.

The sharpness processor provides 1D luminance step improvement and detail enhancement by smart peaking, suitable for both $1f_H$ and $2f_H$ applications. The TDA9177 can be used as a cost effective alternative to (but also in combination with) Scan Velocity Modulation.

An on board 6-bit ADC can be used for interfacing two analogue, low frequency voltage signals to the I^2C-bus .

The supply voltage is 8 Volts. The TDA9177 is mounted in a SDIP-24 envelope.

FEATURES:

- $1f_H$ and $2f_H$ applications
- Luminance step improvement
- Line width control
- Smart peaking for detail enhancement
- Embedded feature reduction facility for smart noise control
- Compensating chrominance delay
- YUV interface
- Two additional pins for access to 6-bit ADC and I^2C-bus
- Versatile I^2C-bus and pin control (DC-voltage control) for user adjustments

CONTENTS

1. Introduction:

In the Television transmission system there are several bandwidth limiting devices from the camera to the picture tube of the Television. The result of all these bandwidth limitation is that the luminance signal has very slow transients from, for instance, white and dark parts of the picture.

The major goal of the TDA9177 is to reconstruct the sharp transients on the expected places on the screen. These transients are detected by the “STEP-DETECTOR”-part of the TDA9177 (see figure 2.0), this part separates transients from detail information in a picture. Depending upon the stepdetector’s result, there are two main functions possible to reconstruct a perceptive sharp picture-part.
First function is the so called ‘Sharpness-control”, this function makes the transients sharper by means of making more gain during the transient.
A second function is the so called ‘Smart Peaking-control’, this function has the goal of making ‘overshoots’ and ‘undershoots’ on a low-to-high transient and on a high-to-low transient in detailed information.

2. Circuit description:

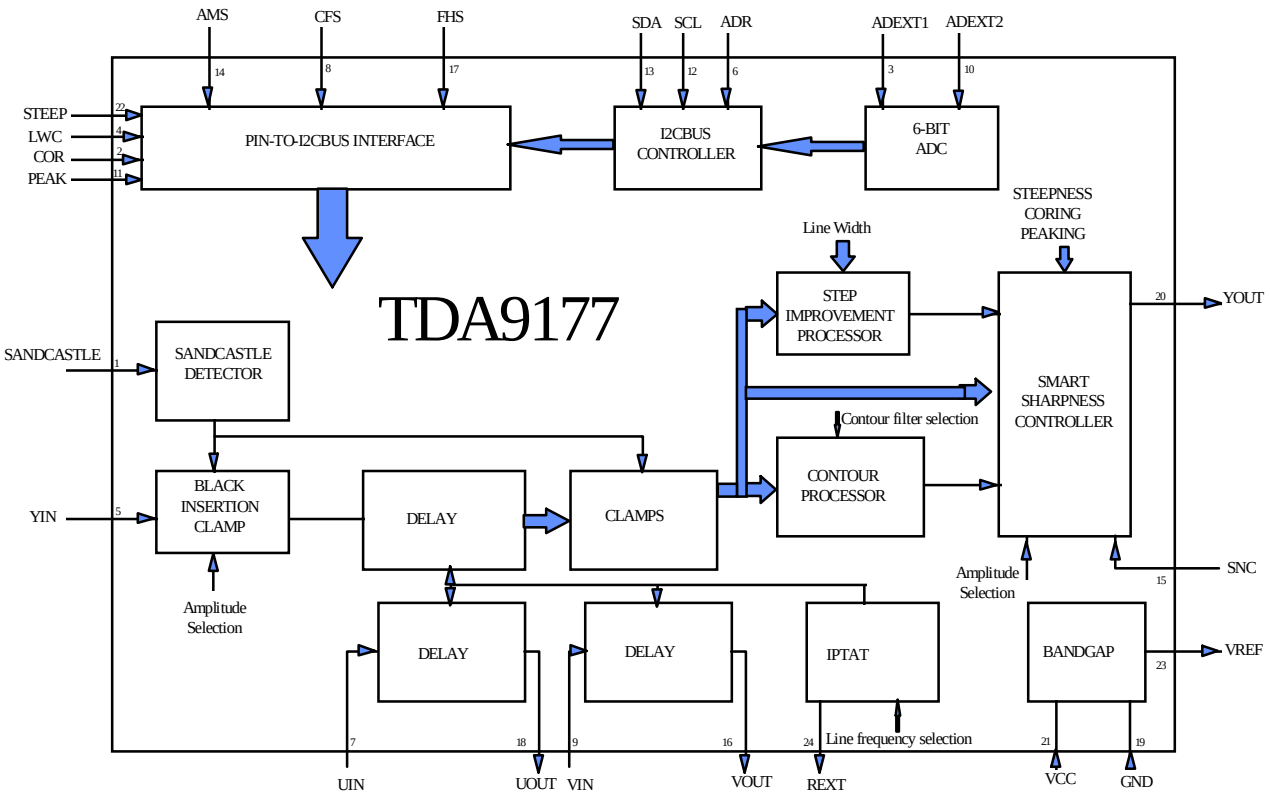


figure 2.0: block diagram TDA9177

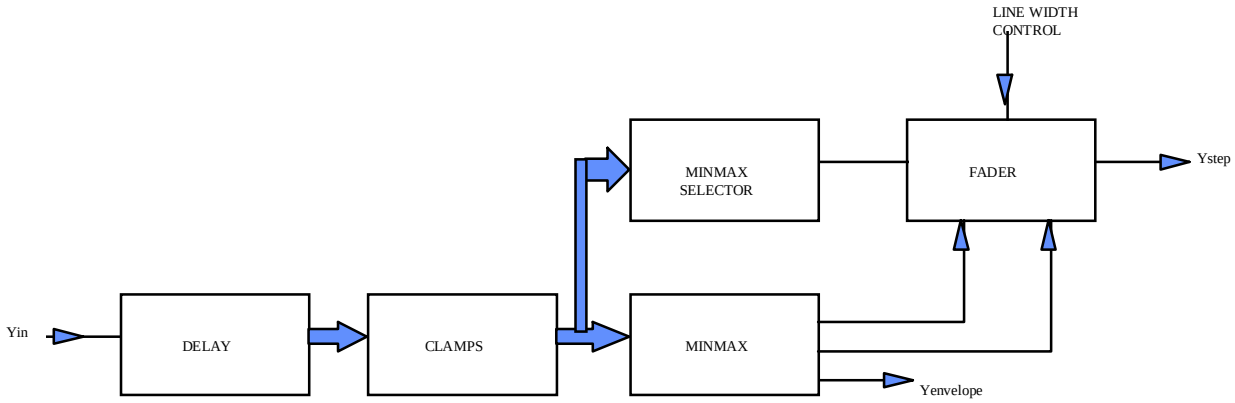
2.1. Y-input selection and amplification

The dynamic range of the luminance input amplifier and output amplifier can de switched between 0.315V and 1.0V typically (excluding sync), either externally (pin AMS) or by I^2C-bus (bit AMS of the control register). Amplitudes exceeding the maximum specified range will be clipped smoothly. The sync part is processed transparently to the output, independently of the feature settings. The input is clamped during the high period of the CLP, defined by the sandcastle reference, and should be decoupled with an external capacitor. During the clamp pulse an artificial black level is inserted in the input signal to correctly preset the internal circuitry. The input amplifier drives a delay line of four delay sections, which forms the core of the Sharpness Improvement Processor.

2.2. Sharpness Improvement processor

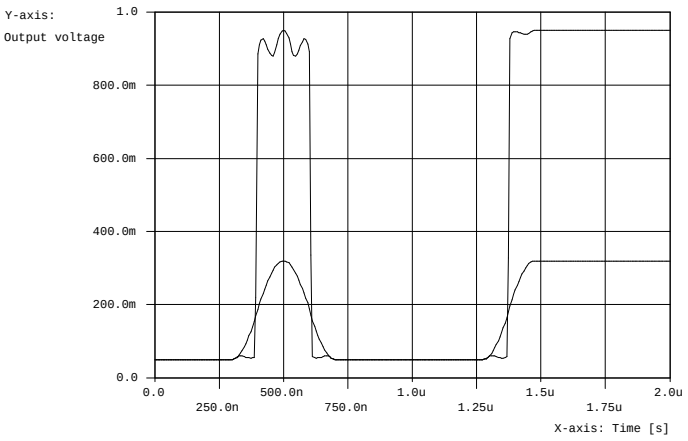
The sharpness Improvement Processor increases the slope of large luminance transients of vertical objects and enhances transients of details in natural scenes by contour correction. It comprises three main processing units, these being the Step Improvement Processor, the Contour Processor and the Smart Sharpness Controller. A description of all circuits is given below.

2.2.1. Step Improvement Processor



The Step Improvement Processor comprises two main functions: the MINMAX generator and the MINMAX fader. The MINMAX generator utilises 5 taps of an embedded luminance delayline to calculate the minimum and maximum envelope of all signals momentarily stored in the delay line. The MINMAX fader chooses between the minimum and the maximum depending on the polarity of a decision signal derived from the contour processor. The MINMAX generator also outputs a signal that represents the momentary envelope of the luminance input signal. This envelope information is used by the Smart Sharpness Controller. **Figures 2.2.1, 2.2.2 and 2.2.3** show some waveforms of the Step Improvement Processor and illustrate that fast transients result with this algorithm.
In **figure 2.2.1** is shown that the Step Improvement Processor does not affect small amplitudes. Large transients however get steeper edges.

Figure 2.2.1: Response signals in case of following settings: Max step improvement, no peaking, nominal linewidth.



Limited line width control (also called aperture control) can be performed externally (pin 4, LWC) or by I²C-bus (LW-DAC). In **figure 2.2.2 and 2.2.3** is shown that the width of the signal processed by the Step Improvement Processor can be modified by the Line Width Control pin LWC (or by I²C-bus: LW-DAC).

Figure 2.2.2: Response signals in case of the following settings: Max step improvement, no peaking, minimal linewidth.

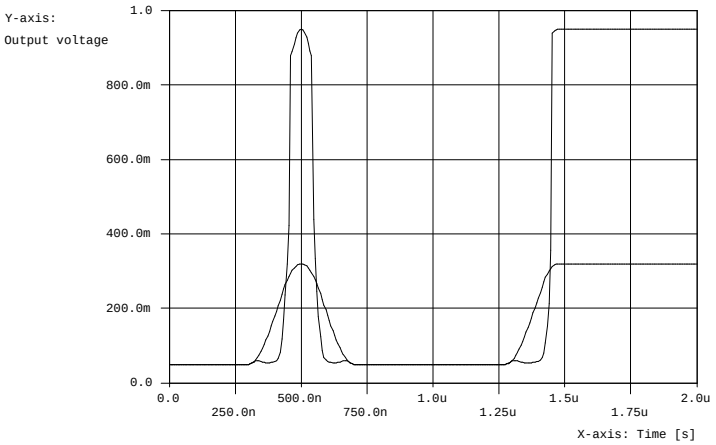
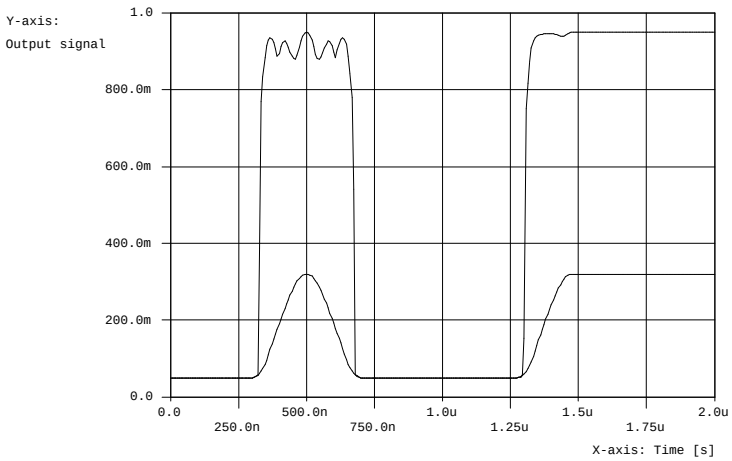
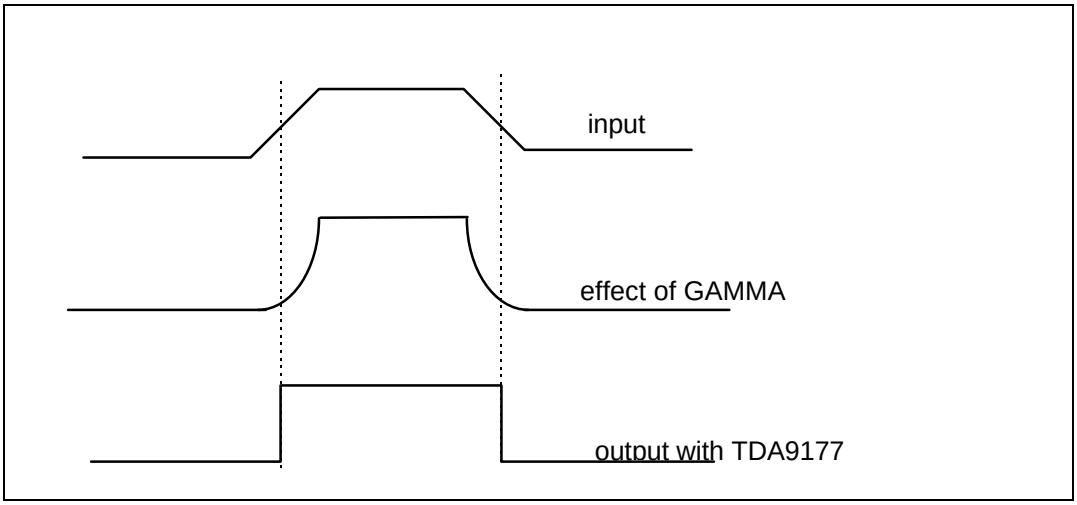


Figure 2.2.3: response signals in case of the following settings: max step improvement, no peaking, maximal linewidth.



Line width control can be used to compensate for horizontal geometry because of the gamma or blooming of the spot of the CRT.

Figure 2.2.4: Change of pulse-width because of Sharpness-control:



Because of the picture-tube gamma, white parts are made smaller (while black parts become larger). However if the input signal is fed to the TDA9177, the gamma no longer plays a role, so the output of this device appears to have larger white areas and smaller black ones. This can be restored by the Line-Width Control function of the TDA9177.

2.2.2. The Contour Processor

The Contour Processor comprises two contour generators with different frequency characteristics. The contour generator generates a second order derivative of the incoming luminance signal and is used both as a decision signal for the Step Improvement Processor and as a luminance correction signal for the Smart Sharpness Controller. In the Smart Sharpness Controller, this correction signal is added to the proper delayed original luminance input signal, making up the peaking signal for detail enhancement. The peaking path is allowed to select either the narrow- or the wide- peaked contour generators either externally (pin CFS) or by I^2C-bus (bit CFS in the control register). The Step Improvement circuitry always selects the wide peaked contour filter. The contour generators utilise 3 taps (narrow band) or 5 taps (broad band) of the embedded luminance delay lines. **Figures 2.2.5 and 2.2.6** illustrate the normalised frequency transfer of both the narrow and wide contour filters.

Figure 2.2.5: Frequency transfers Narrow Contour filter:

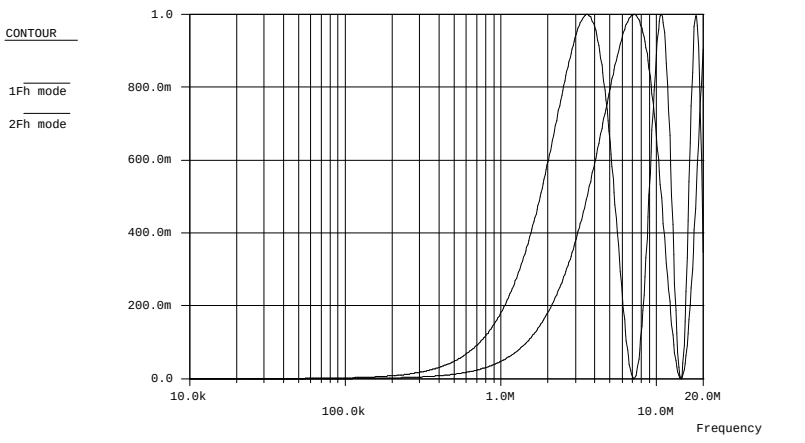


Figure 2.2.6: Frequency transfers Wide Contour filter:

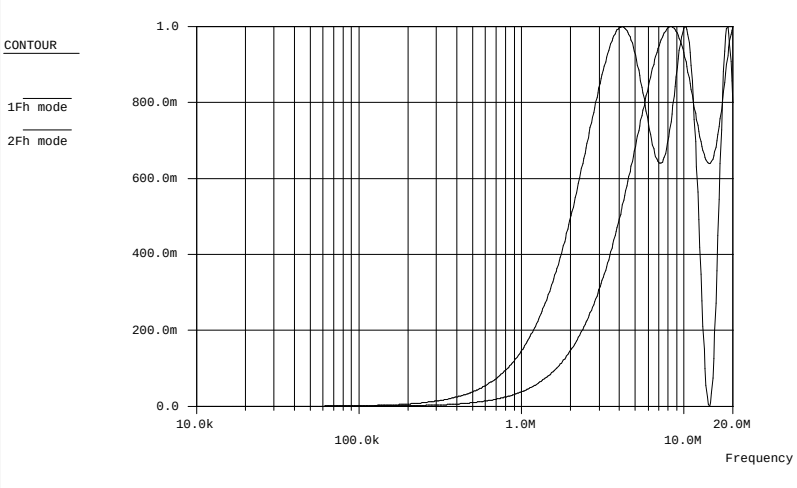


Figure 2.2.7 shows that the contour processor does not affect large transients, but fully works exclusively on small signals, for instance details in a video signal.
Figure 2.2.8 shows the combination of smart peaking and the Step Improvement Processor: small signals will be affected by the contour processor and large transients will be modified by the Step Improvement Processor.

Figure 2.2.7: Response signals in case of the following settings: no step improvement, max peaking, 0% coring.

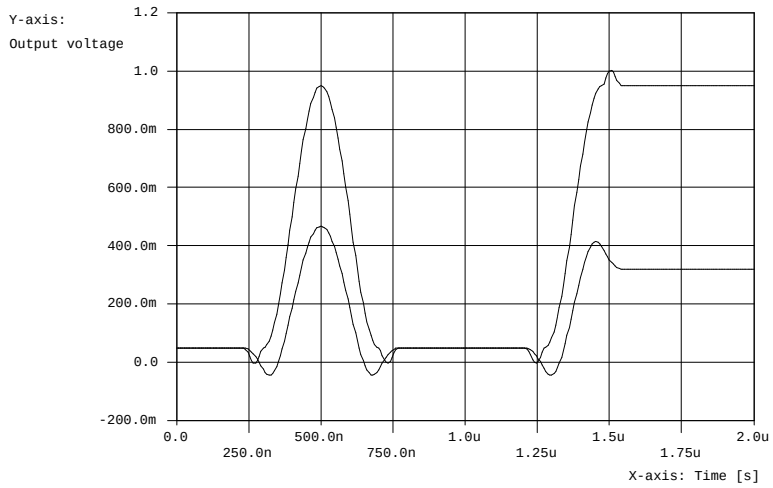
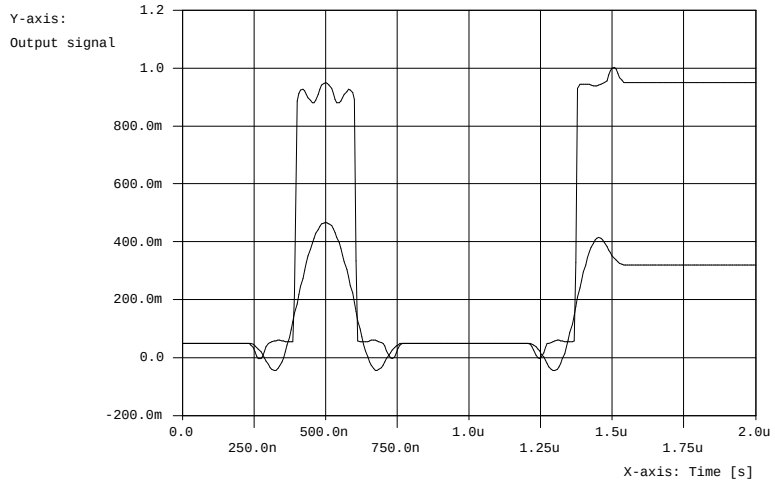
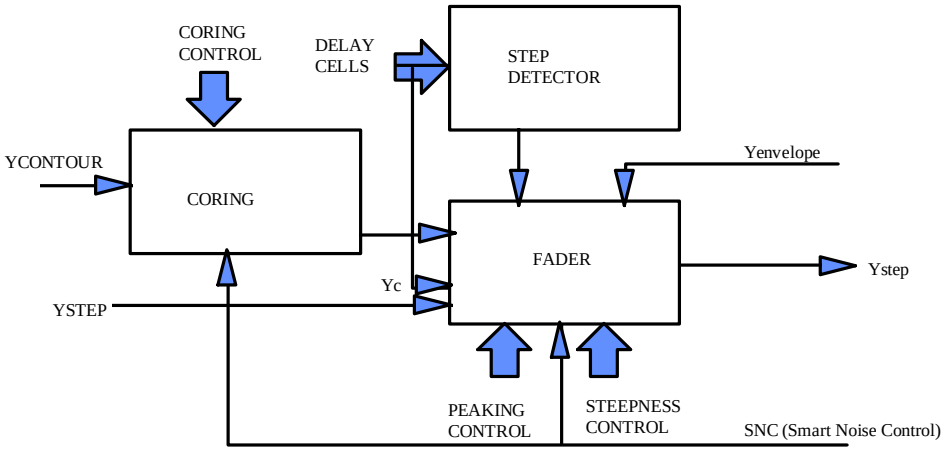


Figure 2.2.8: Response signals in case of the following settings: max step improvement, nominal linewidth, max peaking, 0% coring.



2.2.3. Smart Sharpness Controller

The Smart Sharpness Controller is a fader circuit which fades between peaked luminance and step-improved luminance, defined by the output of a step discriminating device, known as the Step Detector. It also contains a variable coring level stage.



The Step Detector behaves like a bandpass filter, so both amplitude of the step and its slope add to the detection criterion. The Smart Sharpness Controller has four user controls: Steepness control, Peaking control, Coring level control and Smart Noise control. Control settings can be performed either by I^2C-bus or externally by pin depending on the status of the I^2C-bus bit STB.
The steepness setting controls the amount of steepness in the edge correction processing path. The peaking setting controls the amount of contour correction for proper detail enhancement.
The envelope signal generated by the step improvement processor modulates the peaking setting in order to reduce the amount of peaking for large sine excursions.
The coring setting controls the coring level in the peaking path for rejection of high frequency noise. All three settings facilitate reduction of the impact of the sharpness features for instance for noisy luminance signals. An external noise detector (like the one in the TDA9170A), or a user-preferred noise algorithm

are needed to make a fully automatic I²C-bus controlled Smart Sharpness control. An on board, hard-wired Smart Sharpness algorithm can be executed by driving pin SNC with the output of an external noise detector. This pin, however, is active both in I²C-bus and pinmode. **Figures 2.2.9 and 2.2.10** illustrate the impact of the noise control voltage at pin SNC on the user settings.

Figure 2.2.9: Relative decrease of steepness level as function of voltage at pin SNC, starting from four different steepness level presets.

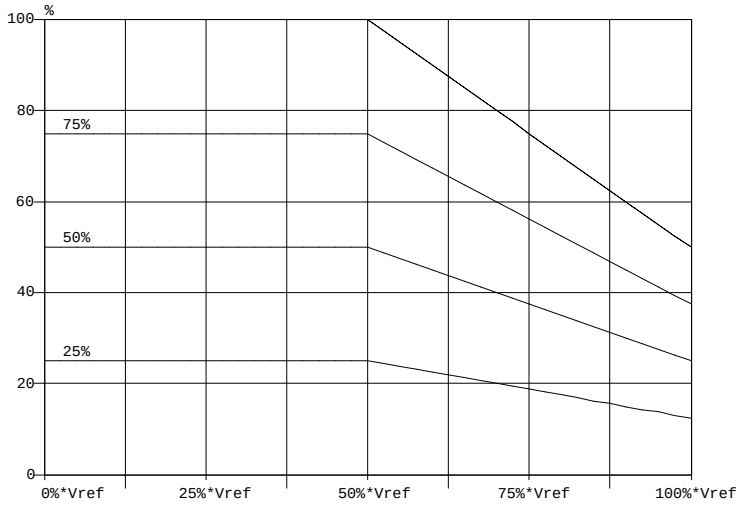


Figure 2.2.10:
Relative increase of coring level as function of pin SNC, starting from different coring level presets

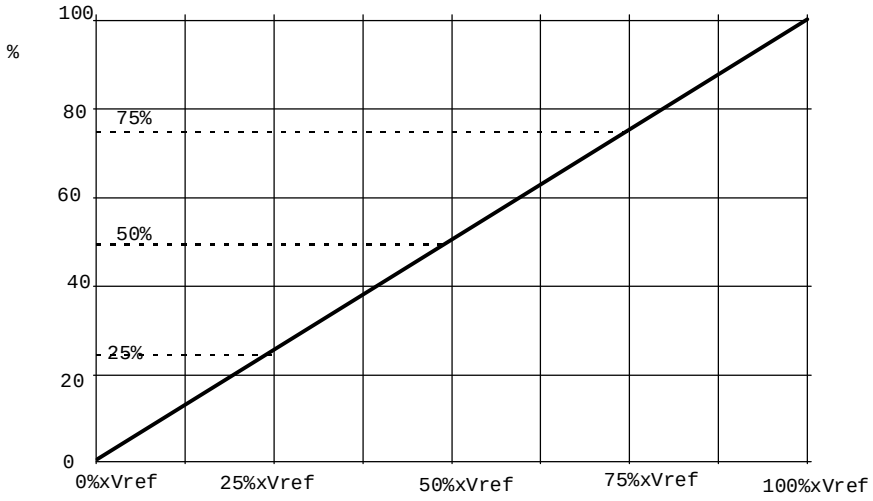
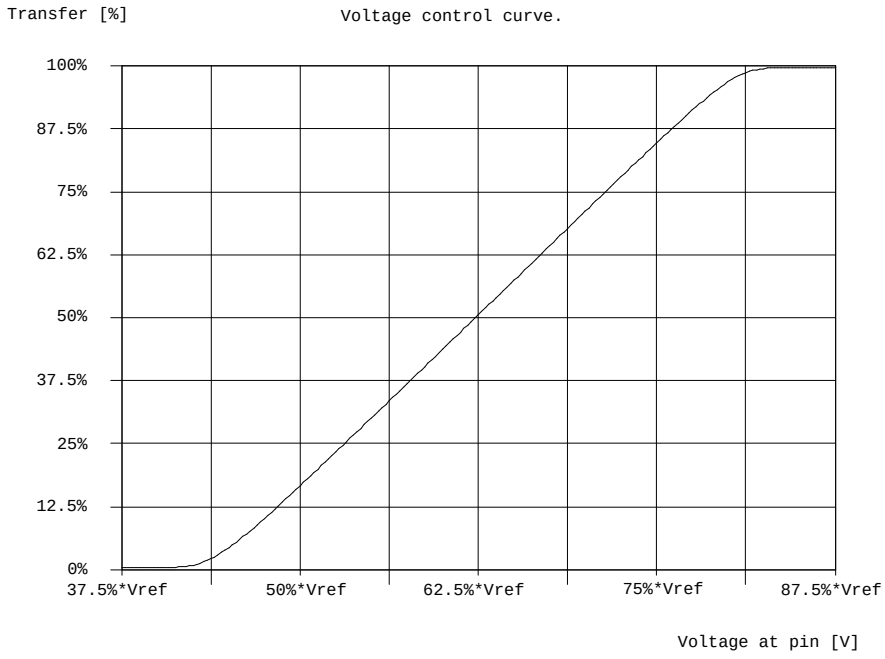


Figure 2.2.11 shows the relationship between the feature settings STEEP, COR, PEAK, LWC and their corresponding pin voltages. The voltages are relative to the reference voltage (Vref), so internal product spread will be compensated in this way.

Figure 2.2.11:
Relationship between feature settings and their corresponding pin voltages:



2.3. Chrominance compensation

The chrominance delay lines compensate for the delay of the luminance signal in the Step Improvement Processor to ensure a correct colour fit. No delay compensation will be performed in the chrominance path for line-width corrections in the luminance path. This is done because of the slow transients in the colour difference signals, it will not be visible on the screen.

2.4. Successive Approximation Analogue to Digital Converter

Pins ADEXT1 and ADEXT2 are connected to a six bit successive approximation ADC via a multiplexer. The multiplexer toggles between the inputs with each field. For each field flyback a conversion is started for either of the two inputs and the result is stored in the corresponding bus register ADEXT1 or ADEXT2. In this way any analog, slowly varying signal can be given access to the I^2C-bus. If a register access conflict occurs, the data of that register is made invalid by setting the flag bit DV (Data Valid) to zero.

2.5. I^2C bus

At power up the bit STB (Standby) in the control register is reset to leave control to the pins. However the I^2C-bus is at standby and responds if properly addressed. By setting STB to logical one, the control of all features is left to the I^2C-bus registers. The PDD bit (Power Down Detected) in the status register is set each time an interruption of the supply power occurs and is reset only by reading the status register. A 3-bit identification code can also be read from the status register, which can be used to automatically configure the application by software. The input control registers can be written sequentially by the I^2C-bus by the embedded automatic subaddress increment feature or by addressing it directly. The output control functions cannot be addressed separately. Reading out the output control functions always starts at subaddress 00 and all subsequent words are read out by the automatic subaddress increment procedure. The I^2C address is 40_{hex} if pin6 (ADR) is connected to ground and $E0_{hex}$ if pin6 (ADR) is connected to pin23 (VREF).

Slave address:

A6	A5	A4	A3	A2	A1	A0	R/W
ADR	1	ADR	0	0	0	0	X

Auto-increment mode available for subaddresses

Control-functions:

INPUTS

	Type	sub-address	databyte D7	D6	D5	D4	D3	D2	D1	D0
Control	REG	00	X	X	X	X	CFS	FHS	AMS	STB
Peaking	DAC	01	X	X	PK5	PK4	PK3	PK2	PK1	PK0
Steepness	DAC	02	X	X	SP5	SP4	SP3	SP2	SP1	SP0
Coring	DAC	03	X	X	CR5	CR4	CR3	CR2	CR1	CR0
Line width	DAC	04	X	X	LW5	LW4	LW3	LW2	LW1	LW0

OUTPUTS

Status	REG	00	0	0	0	0	ID2	ID1	ID0	PDD
ADEXT1 (output)	REG	01	0	DV	AD5	AD4	AD3	AD2	AD1	AD0
ADEXT2 (output)	REG	02	0	DV	AD5	AD4	AD3	AD2	AD1	AD0

Input-signals:

Address selection ADR 0=I^2C-bus address = 40_{hex}
1=I^2C-bus address = $E0_{hex}$

Standby	STB	0=pin mode 1= I^2 C-bus mode	
Amplitude selection	AMS	0= 315mV VIDEO (luminance exclusive sync) 1=1.0 V VIDEO (luminance exclusive sync)	
Line frequency selection	FHS	0= $1f_H$ 1= $2f_H$	
Contour filter selection	CFS	0=Narrow contour filter 1= Wide contour filter	
Peaking amplitude	PK5...PK0		000000= 0% 111111= 100%
Steepness correction	SP5...SP0		000000= 0% 111111= 100%
Coring level	CR5....CR0		000000= 0% 111111= 100%
Line width correction	LW5...LW0		000000= 0% 111111= 100%

Output-signals:

Power Down Detection:	PDD	0= No power down detection since last read action 1= Power down detected

Identification (of version number or derived type):

	ID2	ID1	ID0
TDA9177/N1	0	0	0

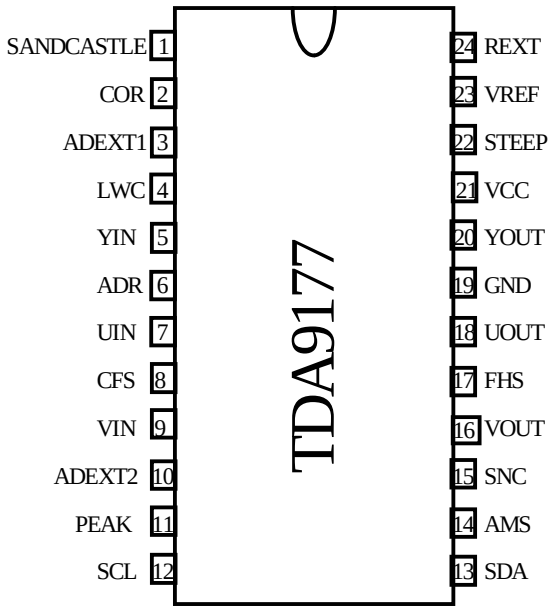
Data Valid of ADC registers	DV	0= Data not valid because of possible register access collision 1= Data Valid
ADC-registers:	AD5...AD0	000000= 0 VOLTS 111111= 0.5*Vref [VOLTS]

Example of register adjustment (Recently used for demonstration purpose)

03 35 37 07 29

(this serves only as an example, the register contents depends upon customers taste and used configuration)

3. **Pinning and external components of the TDA9177:**



Pin	short-name	Description
1	SANDCASTLE	Sandcastle input pulse
2	COR	Coring level control
3	ADEXT1	ADC input #1
4	LWC	Line Width Control
5	YIN	Luminance input signal
6	ADR	I^2C-bus address selection
7	UIN	-(B-Y) input signal
8	CFS	Contour Filter Selection
9	VIN	-(R-Y) input signal
10	ADEXT2	ADC input #2
11	PEAK	Peaking amplitude control
12	SCL	I^2C-bus clock
13	SDA	I^2C-bus data
14	AMS	Amplitude Selection
15	SNC	Smart Noise Control
16	VOUT	-(R-Y) output signal
17	FHS	Line Frequency Select
18	UOUT	-(B-Y) output signal
19	GND	System ground
20	YOUT	Luminance output signal
21	VCC	Supply Voltage
22	STEEP	Steepness control
23	VREF	Reference voltage out
24	REXT	Resistor reference

3.1. Explanation of the pins of the TDA9177:

Pin 1 (Sandcastle):

This input pin is for connecting the required Sandcastle signal, used for deriving the internal timing of the TDA9177.
The TDA9177 is designed for use on both Sandcastle-signals (**2-level sandcastle signal**, or a **3-level sandcastle** signal), The burstkey extraction is realised by TOPDETECTION; the detection-level is 0.6 Volts below the top. The maximum allowable ripple on this burstkey-pulse is 0.4 Vpp.
This means that **no DC-level conversion is necessary**, providing that the blanking level (for line- and frame-information) is higher than the detection-level of the TDA9177 (the detection level of the TDA9177 is between 1.25 and 1.75 volt), and the burstkey pulse is at least 0.8 Volts higher than the blanking level**.**
The input pin has a very high impedance (input current far below 0.5 μA).
The maximum input voltage is limited to 0.6 volts below the supply-voltage.

Pin 2 (Coring control):

This input pin is designed to control the Coring function in case of pin control of the TDA9177.
The input pin has a very high impedance (input current far below 0.5 μA).
The linear coring control curve starts at 37.5% of Vref (about 1.5 Volts), and stops at 87.5% of Vref (about 3.5 Volts). The maximum allowed voltage on this pin is 137.5% of Vref (about 5.5 Volts); see figure 2.2.11.
Because of the quick response from the device to changes in the coring control pin, it is highly recommended to decouple the coring pin with a ceramic capacitor (a good value is 100nF) for suppressing noise and high frequency interference.
When not used (e.g. I^2C-bus control) this should be connected to ground.

Pin 3 (ADEXT1):

This input pin is designed for measuring purpose only, the voltage of this pin will be passed to the I^2C-bus register (e.g. to measure Light Ambient).
The impedance of this pin is high (input current far below 1 μA), and it is designed for low-frequent (DC till $0.5*f_H$) signals.
Testing results are from 0 Volts till 0.5* Vref (about 2 Volts full scale) with a resolution of 6 bit (0 till 63).
The nonlinearity of the measurement is far below 1 LSB.
The maximum voltage at this pin is 5.5 Volts, when this pin is not used it is recommended to short this pin to ground.

Pin 4 (Line Width control):

This input pin is designed to control the Line Width function of the steepness in case of pin control of the TDA9177.
The input pin has a very high impedance (input current far below 0.5 μA).
The linear line width control curve starts at 37.5% of Vref (about 1.5 Volts), and stops at 87.5% of Vref (about 3.5 Volts). The maximum allowed voltage on this pin is 137.5% of Vref (about 5.5 Volts); see figure 2.2.11.
Because of the quick response from the device to changes in the line width control pin, it is highly recommended to decouple the coring pin with a ceramic capacitor (a good value is 100nF) for suppressing noise and high frequency interference.
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 5 (Luminance input):

This input pin is for connection the Y-signal from the Y,U,V-interface.
The input pin has a very high impedance (input current far below 0.1 μA) between the clamping pulses.
This pin must be used in series with a low-leakage clamp capacitor (e.g. MKT-version) of 100nF minimum.
During clamping-time the device expects a low impedant voltage source (Rout < 600 Ohm).
The value of the capacitor determines the clamping performance, a lower capacitor makes faster clamping, but also clamp-noise can occur; a larger capacitor value makes the clamping slow.
All signals below the blanking-time (Sync-pulses) are processed transparently to the output (Y-out, pin20).
During vertical blanking period all features of the TDA9177 are switched off.

During horizontal flyback the features of the TDA9177 are switched off at the beginning of the horizontal blanking till beginning of the burstkey-pule from the sandcastle signal.
The input-signal level can be selected with the AMS-pin (pin 14), or the AMS-selection bit of the I^2C-bus register; a choice can be made between 0.315 Volts video (black to White, excluding sync) and 1.0 Volts video (black to white, excluding sync).

Pin 6 (I^2C-bus address selection):

This input-pin is designed to set the address of the I^2C-bus interface to either 40_{HEX} (pin6=low) or $E0_{HEX}$ (pin6=high).
The input impedance is very high.
A voltage below 0.5 Volts selects address 40_{HEX}, and a voltage above 3.5 volts selects address $E0_{HEX}$.
The maximum allowed voltage at this pin is 5.5 Volts.
When not used (e.g. when de TDA9177 is in pin-control) it is recommended to connected this pin to ground.

Pin 7 (colour difference input U_IN):

This input pin is for connection the U-signal from the Y,U,V-interface.
The input pin has a very high impedance (input current far below 0.1 μA) between the clamping pulses.
This pin must be used in series with a low-leakage clamp capacitor (e.g. MKT-version) of 10nF minimum.
During clamping-time the device expects a low impedant voltage source (Rout < 600 Ohm).
The value of the capacitor determines the clamping performance, a lower capacitor makes faster clamping, but also clamp-noise can occur; a larger capacitor value makes the clamping slow.
The TDA9177 can handle input signals upto 1.9 Volts pp.

Pin 8 (contour filter selection):

This input is designed to select one of the available contour filters in case of pin-control of the TDA9177.
The input-impedance is high (1MOhm to ground internally).
A voltage level below 0.5 volts selects the narrow-filter, and a voltage above 3.5 Volts selects the wide-filter.
The maximum allowed voltage at this pin is 5.5 volts.
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 9 (colour difference input V_IN):

This input pin is for connection the V-signal from the Y,U,V-interface.
The input pin has a very high impedance (input current far below 0.1 μA) between the clamping pulses.
This pin must be used in series with a low-leakage clamp capacitor (e.g. MKT-version) of 10nF minimum.
During clamping-time the device expects a low impedant voltage source (Rout < 600 Ohm).
The value of the capacitor determines the clamping performance, a lower capacitor makes faster clamping, but also clamp-noise can occur; a larger capacitor value makes the clamping slow.
The TDA9177 can handle input signals upto 1.9 Volts pp.

Pin 10 (ADEXT2):

This input pin is designed for measuring purpose only, the voltage of this pin will be passed to the I^2C-bus register (e.g. to measure Light Ambient).
The impedance of this pin is high (input current far below 1 μA), and it is designed for low-frequent (DC till $0.5*f_H$) signals.
Testing results are from 0 Volts till 0.5* Vref (about 2 Volts full scale) with a resolution of 6 bit (0 till 63).
The nonlinearity of the measurement is far below 1 LSB.
The maximum voltage at this pin is 5.5 Volts, when this pin is not used it is recommended to short this pin to ground.

Pin 11 (Peaking control):

This input pin is designed to control the Peaking amplitude in case of pin-control of the TDA9177.
The input pin has a very high impedance (input current far below 0.5 μA).
The linear line width control curve starts at 37.5% of Vref (about 1.5 Volts), and stops at 87.5% of Vref (about 3.5 Volts). The maximum allowed voltage on this pin is 137.5% of Vref (about 5.5 Volts); see figure 2.2.11.

Because of the quick response from the device to changes in the peaking control pin, it is highly recommended to decouple this pin with a ceramic capacitor (a good value is 100nF) for suppressing noise and high frequency interference.
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 12 (I^2C-bus clock):

This input-pin is designed for the I^2C-bus controller's clock-pulse.
The input impedance and input amplitudes are conform the I^2C-bus definition.
It is recommended to use 100 Ohm series resistance conform the definition.
When not used (e.g. when de TDA9177 is in pin-control) this pin can be connected to ground.

Pin 13 (I^2C-bus data):

This input/output-pin is designed for the I^2C-bus controller's data-pulse.
The input impedance and input amplitudes are conform the I^2C-bus definition.
It is recommended to use 100 Ohm series resistance conform the definition.
When not used (e.g. when de TDA9177 is in pin-control) this pin can be connected to ground.

Pin 14 (Amplitude selection):

This input-pin is designed for selecting the amplitude of the Luminance signal at pin 5 (Y-IN) in case of pin-control of the TDA9177.
The input impedance is high (1MOhm to ground internally).
A voltage level below the 0.5 volts selects the lower luminance range (0.315 V video), and a voltage level above 3.5 volts selects the higher range (1.0 V video).
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 15 (Smart Noise Control):

This input pin is designed for reducing the amount of features (modulating the Steepness and Coring) of the currently setted values (pin-control and I^2C-bus control). Zero voltage at this pin means: no reduction (maximum Steepness and minimum Coring) and maximum voltage means: maximum reduction (minimum Steepness and maximum Coring) of the TDA9177 performance.
The input pin has a high impedance (input current far below 1 μA).
The linear Smart Noise Control curve starts at zero voltage, and stops at Vref (100%, about 4 Volts). The maximum allowed voltage on this pin is 137.5% of Vref (about 5.5 Volts); see figure 2.2.10.
Because of the quick response from the device to changes in the SNC pin, it is highly recommended to decouple this pin with a ceramic capacitor (a good value is 100nF) for suppressing noise and high frequency interference.
When this pin is not used it is recommended to short this pin to ground.

Pin 16 (Colour difference V_out):

This is a output pin of the TDA9177.
The output impedance is about 100 Ohm.
The voltage level during blanking is about 3.2 Volts.
There is no amplification or attenuation with respect to the input signal (V_IN, pin 9), only delay-compensation with respect of the Luminance signal is performed.
Any capacitance load to this pin can reduce the bandwidth of this colour-difference signal .
With a capacitance load of 15 pF maximum, the bandwidth in $1f_H$ and in $2f_H$ is more than 7 Mhz.
If input-signals have frequency components above 4 MHz, "ringing" may occur, due to imitations of the internal all-pass filter.

Pin 17 (Line Frequency Selection):

This input-pin is designed to set the linefrequency of the TDA9177 to either $1f_H$ or $2f_H$ in case of pin-control of the TDA9177.
The input impedance is very high (1MOhm to ground internally).
A voltage below 0.5 Volts selects the $1f_H$ frequency operation, and a voltage above 3.5 volts selects the $2f_H$ frequency operation.

The maximum allowed voltage at this pin is 5.5 Volts.
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 18 (colour difference U_out):
This is a output pin of the TDA9177.
The output impedance is about 100 Ohm.
The voltage level during blanking is about 3.2 Volts.
There is no amplification or attenuation with respect to the input signal (U_IN, pin 7), only delay-compensation with respect of the Luminance signal is performed.
Any capacitance load to this pin can reduce the bandwidth of this colour-difference signal .
With a capacitance load of 15 pF maximum, the bandwidth in $1f_H$ and in $2f_H$ is more than 7 MHz.
If input-signals have frequency components above 4 MHz, “ringing” may occur, due to imitations of the internal all-pass filter.

Pin 19 (ground connection):

This pin is the ground reference of the TDA9177, connection to the system-ground and to decoupling capacitors for the supply voltage should have short connections.

Pin 20 (Luminance output):

This is a output pin of the TDA9177.
The output impedance is about 100 Ohm.
The output-signal level can be selected with the AMS-pin (pin 14), or the AMS-selection bit of the I^2C-bus register; a choice can be made between 0.315 Volts video (black to White, excluding sync) and 1.0 Volts video (black to white, excluding sync).
The voltage level during blanking is about 2.35 Volts in the lower input signal range (AMS=low), and 2.0 Volts in the higher input voltage range (AMS=high).
The delay of this output signal w.r.t. the input signal is about 175 nSEC ($1f_H$) or 108 nSEC ($2f_H$).
The bandwidth of the luminance path is at least 10 MHz in $2f_H$- and 5 MHz in $1f_H$- mode.
As this output signal has improved transients, the bandwidth of this signal is very much higher than the normal luminance signal.
Any capacitance load to this pin can reduce the bandwidth of this luminance output signal (the bandwidth is granted with a maximum capaciance load of 15 pF).

Pin 21 (Vcc):

This pin is the supply-voltage pin of the TDA9177, connection with a decoupling capacitors to ground should have short connections (recommended is a ceramic capacitor of 100 nF with a electrolytic capacitor of 100 uF).
The nominal voltage is 8.0 Volts (range: 7.2 till 8.8 Volts), and the nominal current drawn from 8.0 Volts is about 40 mA in $1f_H$- and 45 mA in $2f_H$- mode.

Pin 22 (Steepness control):

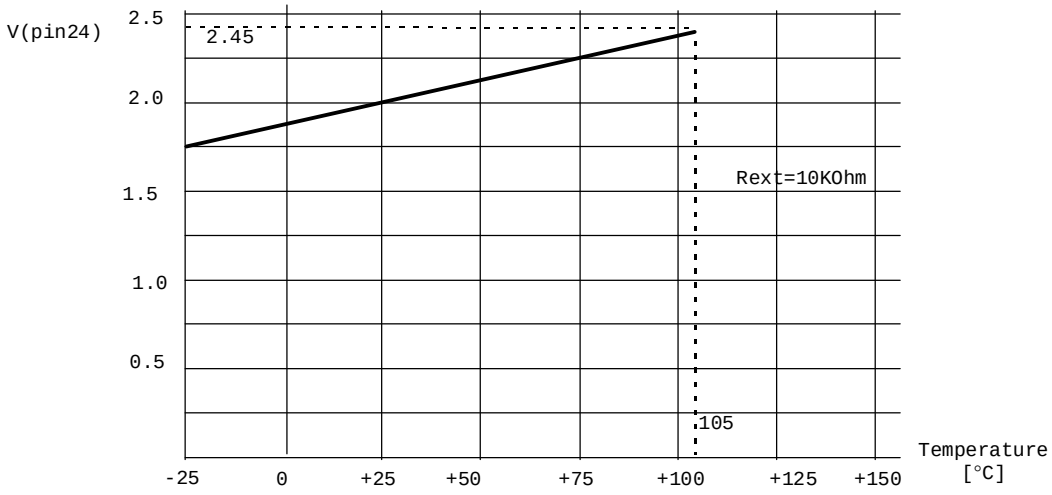
This input pin is designed to control the Steepness amplitude in case of pin-control of the TDA9177.
The input pin has a very high impedance (input current far below 0.5 μA).
The linear line width control curve starts at 37.5% of Vref (about 1.5 Volts), and stops at 87.5% of Vref (about 3.5 Volts). The maximum allowed voltage on this pin is 137.5% of Vref (about 5.5 Volts); see figure 2.2.11.
Because of the quick response from the device to changes in the peaking control pin, it is highly recommended to decouple this pin with a ceramic capacitor (a good value is 100nF) for suppressing noise and high frequency interference.
When not used (e.g. I^2C-bus control) this pin can be connected to ground.

Pin 23 (Vref):

This output pin is the internal made reference voltage level for the TDA9177 in use, all linear control functions in pin-control of the TDA9177 should be derived from this voltage (potmeters or resistor-dividers), so that the control curves have a compensation for sample-spread. All switching input pins (CFS, FHS, AMS and ADR) can be directly connected to this pin.
It is recommended to add a ceramic decoupling capacitor of about 100nF to this pin with short connections to the ground pin when the TDA9177 is in pin-mode, to reduce high frequency components; when using the I^2C-bus mode, this capacitance can be omitted.
The maximum current drawn from this pin is allowed to be 1mA, and the nominal voltage at this pin is 4.0 Volts.

Pin 24 (Resistor reference):

This pin is designed for an external resistor of 10 Kohm, for use as an internal reference for the TDA9177.
Take care not to connect any capacitor to this pin, this will result in producing noise in the Luminance output signal; the resistor should have a short connection to the ground pin.
The voltage level of this pin is about 2 Volts (due to a 200µA current source), and **strongly depends on the temperature** (this is the internal temperature-compensation voltage).



This reference current is used to adjust several internal actions (as peaking frequency's, delay, filter settings and more).

3.2. Internal pin description:

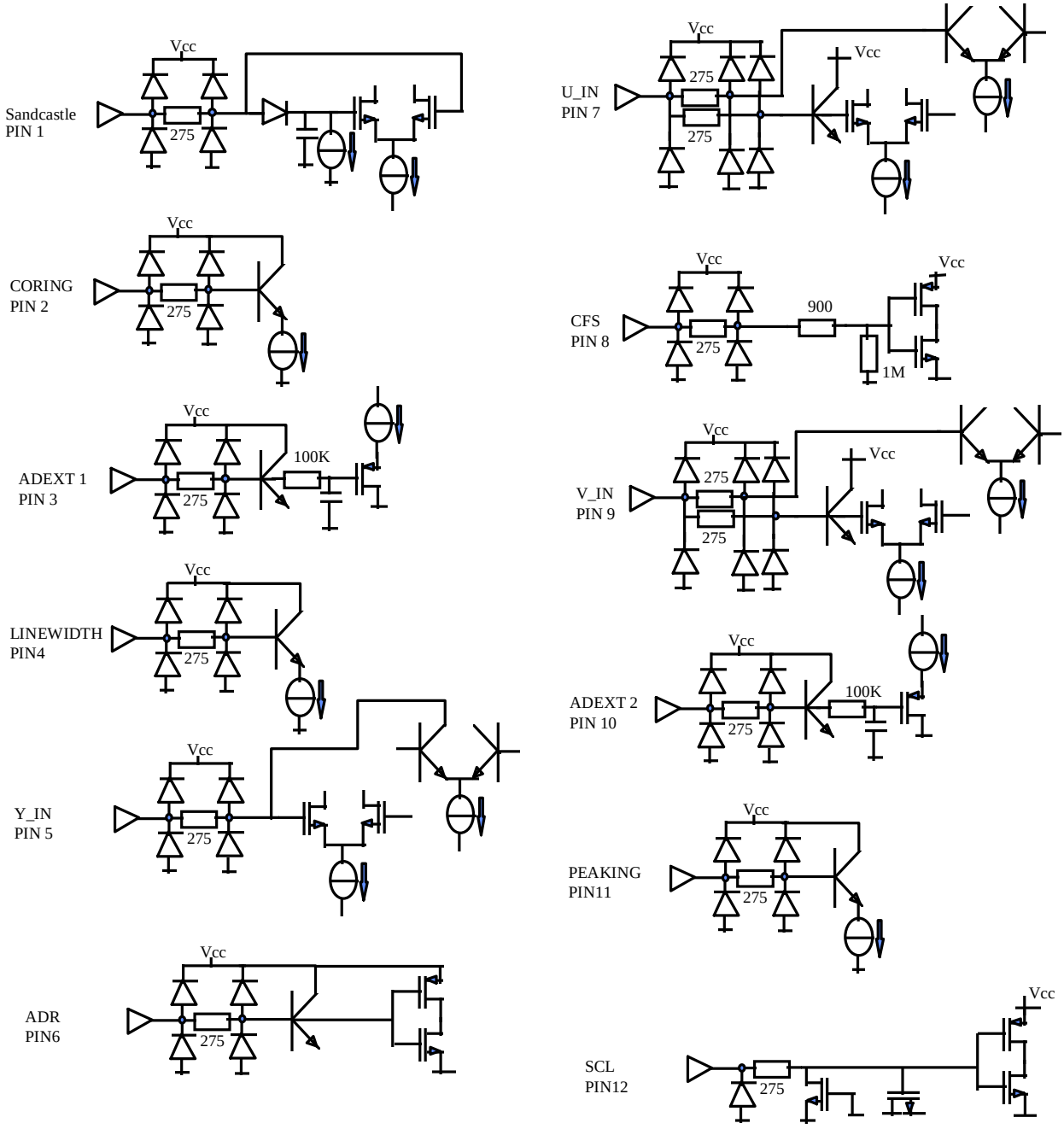


Figure 3.2.1 : Simplified circuit diagrams pin1 till pin12

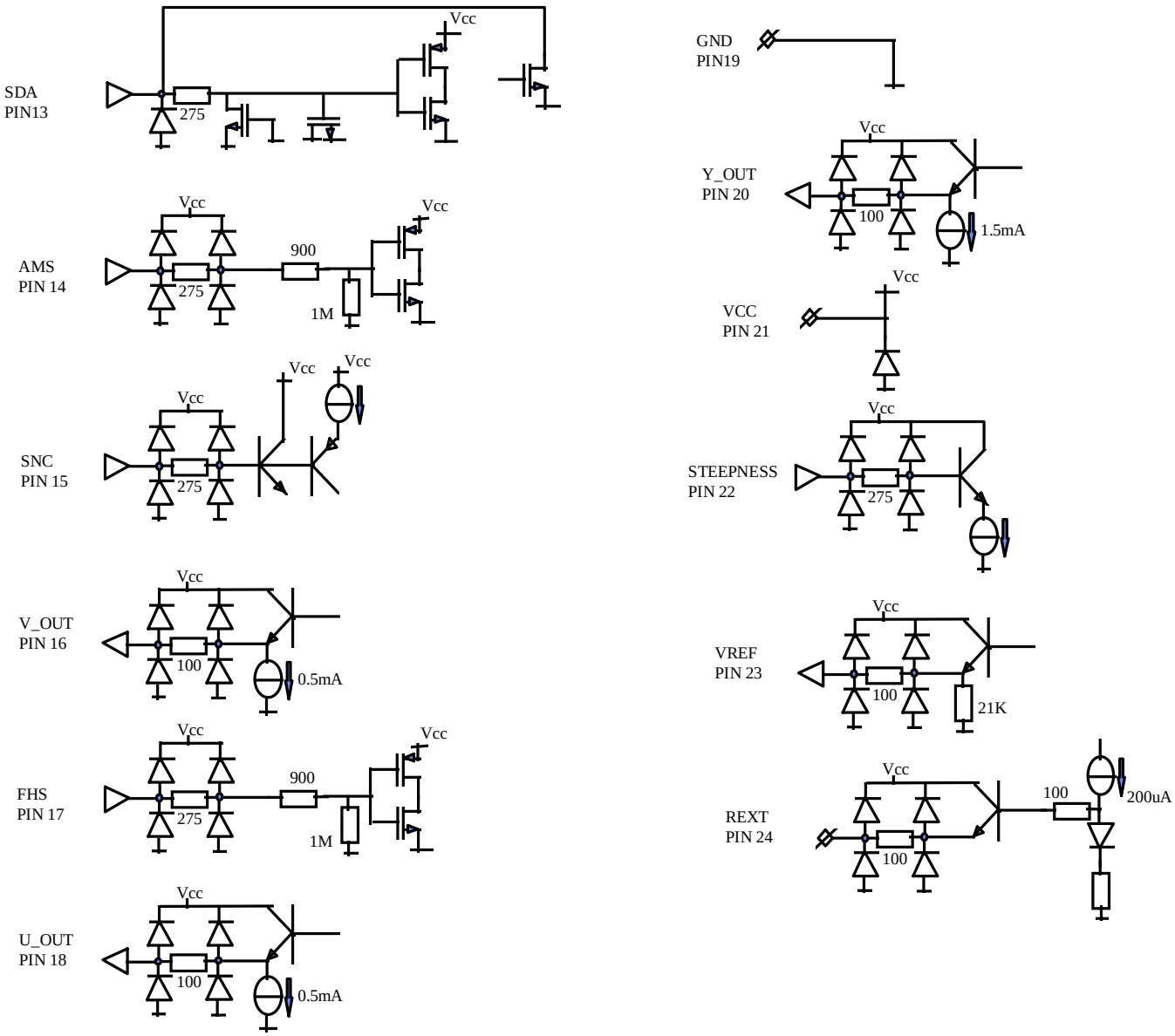
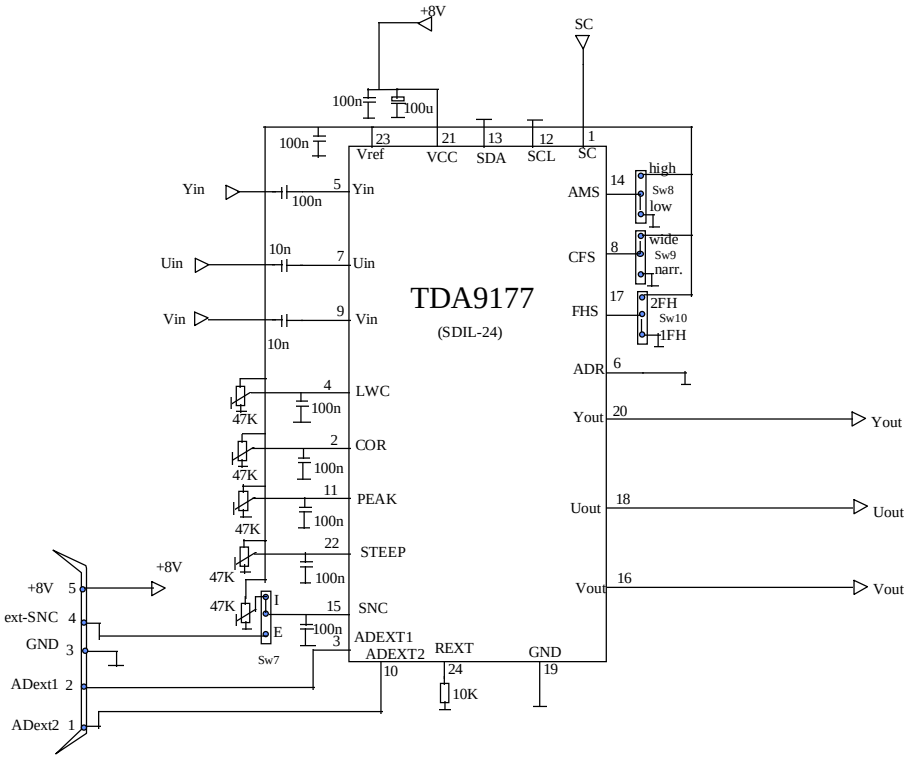
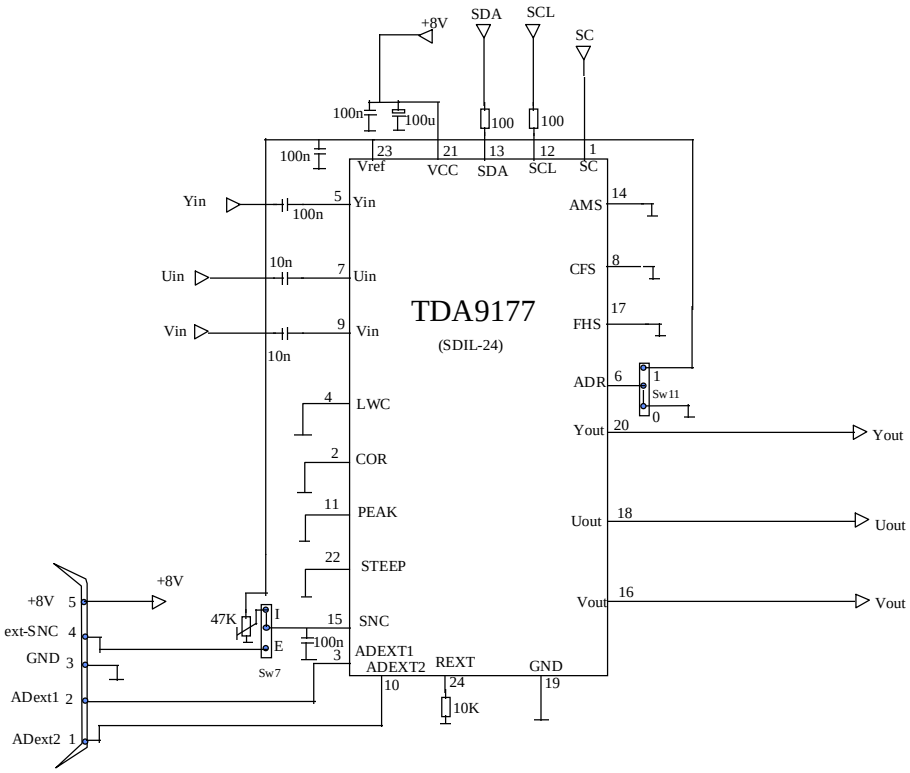


Figure 3.2.2 : Simplified circuit diagrams pin13 till pin24

3.3. External components (manual mode):



3.4. External components (I²C-bus mode):



4. **The DEMO-BOARD (7322-442-27001):**

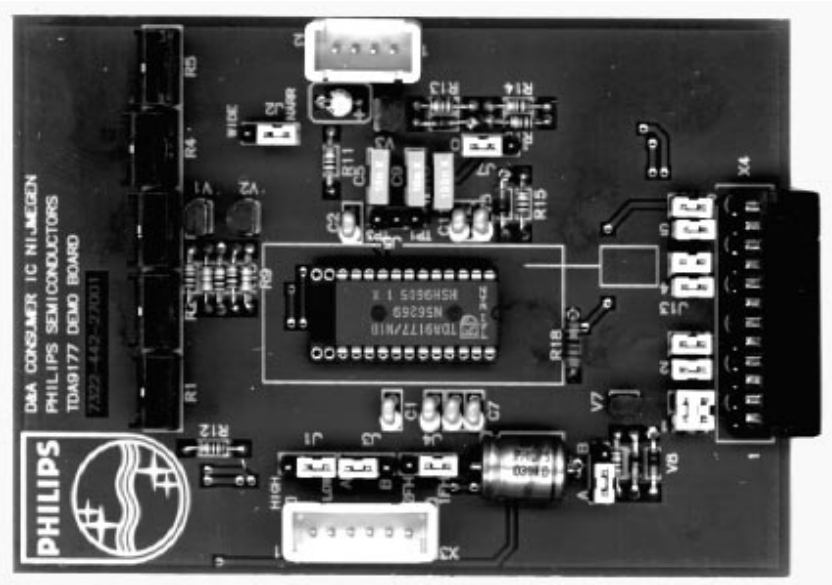


PHOTO1: Component-Side

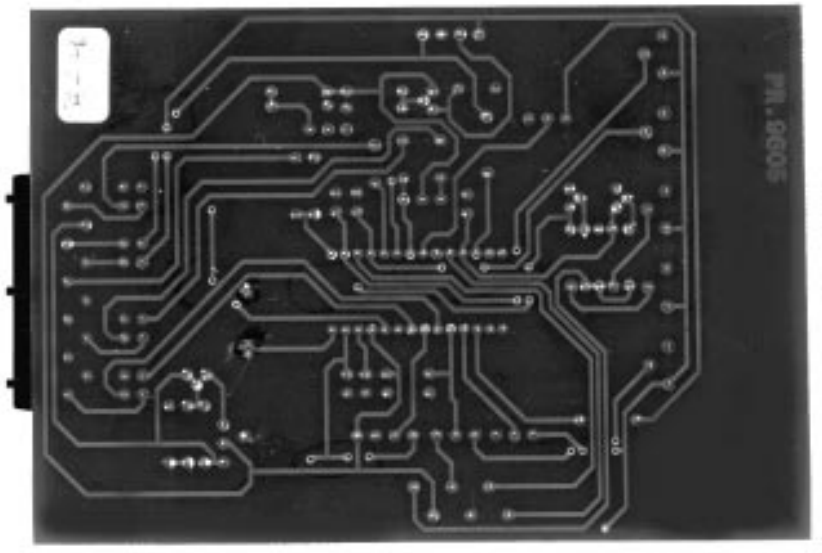
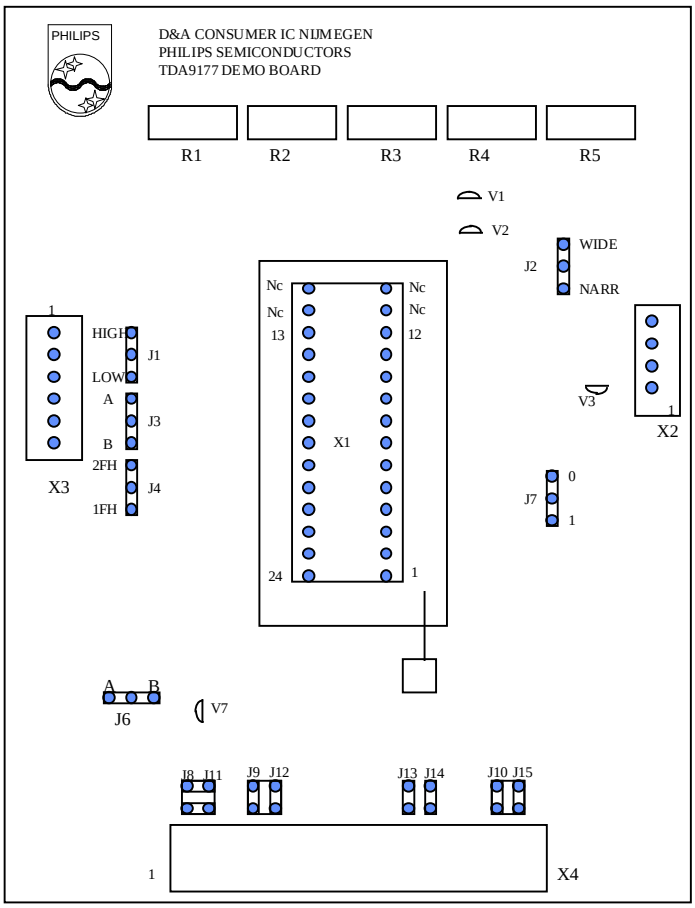
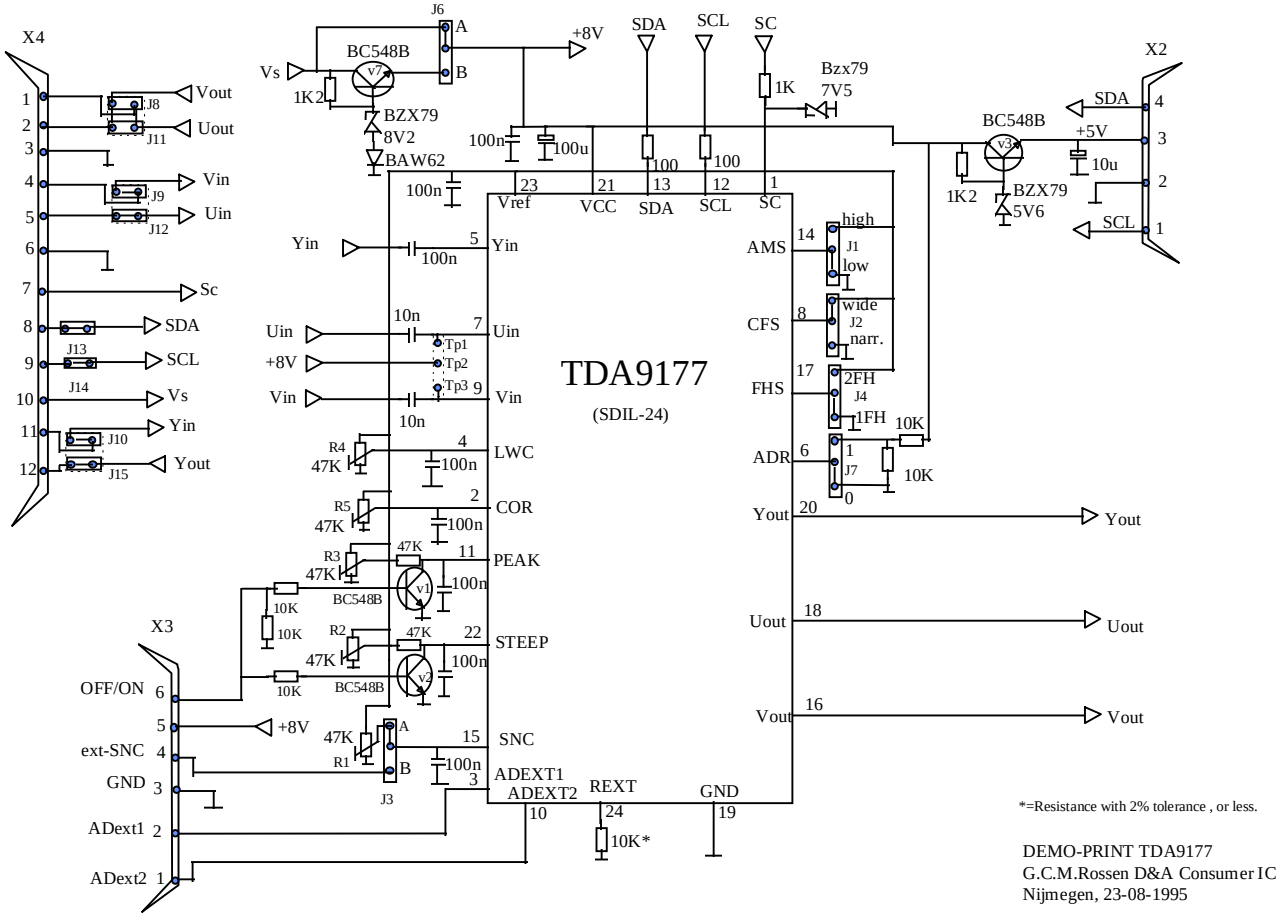


PHOTO2: Soldering-Side

4.1. LAYOUT DEMO BOARD (FIGURE 4.1.1):



4.2. ELECTRICAL DIAGRAM DEMO-BOARD (FIGURE 4.2.1):



4.3. INPUT SIGNALS:

The DEMO-board is provided with a zener diode to make sure the sandcastle-signal to the TDA9177 is limited to 8 Volts. The series resistance (1K) with the sandcastle signal, together with the zener diode (BZX79C-7V5) is only required for the 3-level sandcastle pulse (based on 12 Volts), a 2 level sandcastle signal can be connected directly to pin1.

The signal for the **U-amplifier (-(B-Y) signal)** is expected to lie within 0...1.9 Volts pp (typical 1.33 Volts for a standard EBU-pattern colour bar with 75% saturation).

The signal for the **V-amplifier (-(R-Y) signal)** is expected to lie within 0..1.9 Volts pp (typical 1.05 Volts for a standard EBU-pattern colour bar with 75 % saturation).

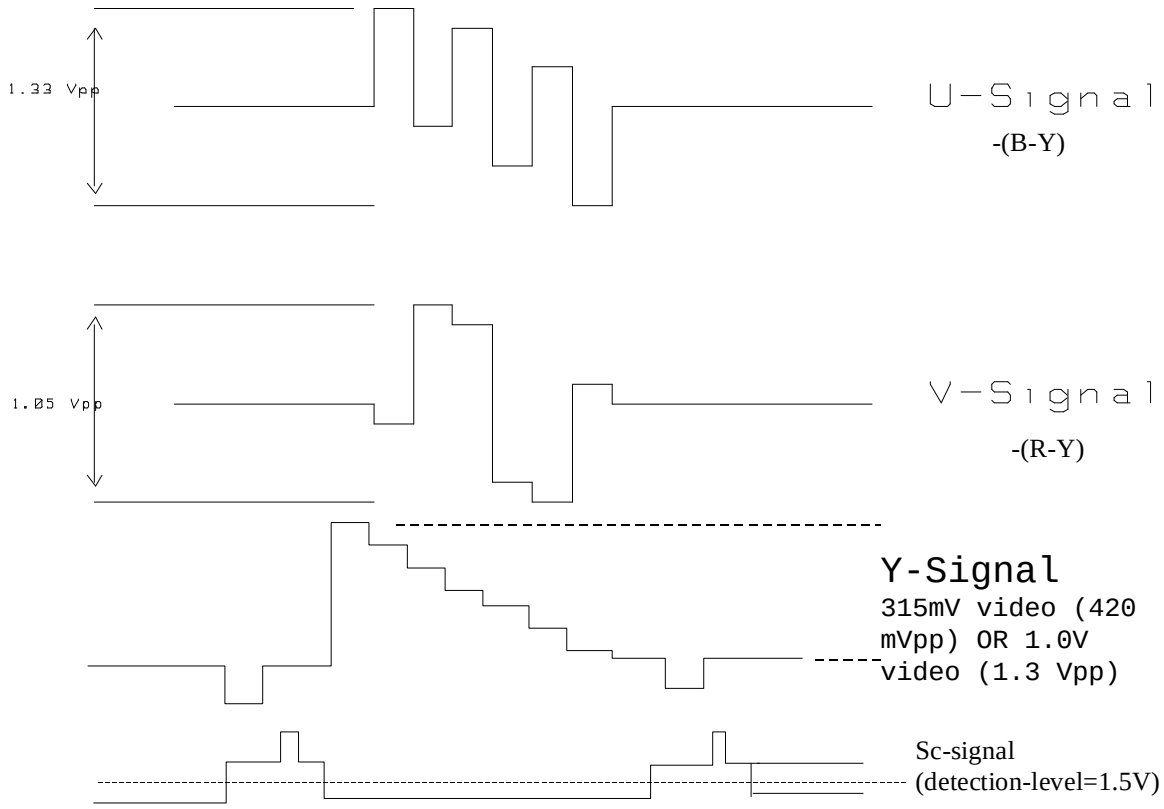


FIGURE 4.3.1.

4.4. CHOICE OF COMPONENTS:

All resistance's, except for REXT at pin24, in the DEMO-board are with 5% tolerance (SFR16T-series,2322-180-73xxx).
The resistance REXT at pin24 of the TDA9177 determines the PEAKING-frequencies; internal spread of the device grants the values according to the specification. The spread of this resistance is increasing the spread in the peaking frequencies, and therefore we recommend to use a 2% tolerance version or better.

Capacitors (not electrolytic) for clamping (pins 5,7,9 of the TDA9177) are low leakage-types (MKT-series, 2322-371-21xxx).
Capacitors (not electrolytic) for decoupling purpose are ceramic types.
All electrolytic capacitors are 16 Volts types.

Decoupling capacitors must be connected close to the IC-pins.
There must be a short connection of the REXT (pin24 resistance) to the ground (pin19).

The maximum current drawn from the reference pin (pin23) must always be below 1.0 mili-Amps to grant a good performance of the TDA9177.

4.5. SETUP OF JUMPER POSITIONS ON DEMO-BOARD

The YUV-connector (X4):

For the YUV-connector (X4), there are three **jumper sets (J10/J15,J9/J12 and J8/J11**) which are designed to make the YUV-interface compatible with main-boards.

For instance if this demo-board is placed upon the ONE-CHIP application board (e.g. TDA8375) the Yin and Yout must be exchanged, therefore the jumpers on the **jumper-set J10/J15** must be disconnected, turned 90 degrees and placed back again.
Jumper-sets (J9/J12 and J8/J11) are for eventual exchanging the U- and V-signals in case the signals being switched on the connector (the TDA9177 treats the U- and V-signals in the same way, so there is no need to exchange these signals).

The I^2C-bus :

When the TDA9177 will be used with I^2C-bus control, and the I^2C-bus signals are not present on the YUV-connector, the **jumpers J13 and J14** must be removed. Now the **I^2C-bus interface of connector X2** can be used.

The supply-voltage:

When the YUV-interface has 12 Volts on pin10 , the **jumper of J6** must be set in position 'B', in stead of position 'A', which is for normal 8 Volts supply.

Smart-Sharpness-control:

When there is an external Smart-Sharpness circuit available to work with the TDA9177, the **jumper J3** must be set in position 'B' and the "SNC"-signal can be applied to pin4 of connector X3, otherwise the potentiometer R1 can be used as Smart-Sharpness control and the jumper must be set in position 'A'.

The configuration settings:

When the Yin-signal is 1.3 Volts-peak-peak (1.0 Volts video) the **jumper J1** must be set in position 'high', else the TDA9177 expects 420 mV peak-peak (315 mVolts video), and the jumper is in position 'low' (which is the default position).

When the TDA9177 must use a wide contour-filter, the **jumper J2** must be placed in position 'wide' (which is the default position), else the jumper must be in position 'narr' to use the narrow contour filter.

When the TDA9177 is going to be used in an $2f_H$ (100 Hz application) the **jumper J4** must be set to position '2FH', else the $1f_H$ (50 Hz application) is selected when the jumper is in position '1FH' (which is the default position).

The slave-address for the I^2C-bus control of the TDA9177 is set to $E0_{HEX}$ when **jumper J7** is set to position '1', else the slave address is 40_{HEX} when sw11 is set to position '0' (which is the default position).

Miscellaneous:

The point **Tp1, Tp2 and Tp3 are only TESTPOINTS**, there is no jumper placed on these pins!!

4.6. RECOMMENDED ADJUSTMENT PROCEDURE

Start with all potentiometers at minimum (take care, the SNC-potentiometer turns in opposite direction for minimum).

Apply a MULTIBURST input signal

1. Turn the STEEPNESS-potentiometer (R2) for sharp bars in the 1.5 MHz part of the multiburst, adjust for acceptable jitter in the bars.
2. Control the LINEWIDTH-potentiometer (R4) for equal width of the bars (white/black= 50%) in the 1.5 MHz part.

Apply an EBU-testpattern.

3. Control the PEAKING-potentiometer (R3) for a sharp picture.
4. Control the CORING-potentiometer (R5) for suppression of the background-noise.
5. Repeat step 3/4 until picture is acceptable (the coring reduces the effect of peaking).
6. The potentiometer R1 is for future applications (SMART-NOISE Control), leave this at minimum (zero voltage at pin15 of the TDA9177).

4.7. THE EXTERNAL CONNECTOR (X3):

The external connector (X3) is designed for some special signals for the TDA9177.

It is recommended to short-circuit pins 1 and 2 to ground (pin3), when the AD-converter inputs (Adext1 and Adext2) are not used.

When there is no external Smart-Sharpness (SNC) control available it is recommended to use the potentiometer (R1) of the demo-board, and to set switch J3 in position 'A'. But a external signal can be applied to pin4 if available.

When pins 6 and 5 are short-circuited, the TDA9177 switches to transparant-mode (no features active), so connecting a switch between these pins, a fast on/off view of the functionality of the TDA9177 is possible when no I^2C-bus control is used (PIN-mode).

5. General application information of the TDA9177:

Because this IC is realised in BIMOS technology, all the normal precautions are to be taken when handling the device.

The application of the TDA9177 is very easy to implement in a TV-set due to the transparent YUV-YUV interface and the need for only one timing signal: a Sandcastle pulse. With transparency is meant that in linear mode the TDA9177 acts as a shortcut for the YUV signals.

The TDA9177 is a stand-alone chip for analogue and time continuous picture improvement, and no clock signals (external or internally generated) are used.

As the TDA9177 uses all-pass filters, “ringing” of the output signals (Y/U/V-output) may occur if the bandwidth of the input signals (Y/U/V-input) are larger than the bandwidth of the circuit (see ‘explanation of the pins’).

As the TDA9177 adds harmonics to the luminance signal, the bandwidth of the luminance output signal is much larger than the bandwidth of the input signal.

For a proper colour compensation the time delay between the luminance (Y) and the colour difference input signals (U and V) should not supersede the requirements of the set, e.g. 40 ns. In case of more delay, artificial colour transients may become visible and correction of this delay is necessary.

The information about the black level has to be in the YUV signals (backporches) to ensure the clamping action of the TDA9177.

If the Automatic Beam Limiter (ABL) is in action this circuit can counteract the actions of the TDA9177 and reduce the performance.

5.1. Place of the TDA9177 in a TV-set:

Because of the high frequency components of the improved step-functions, the place of the TDA9177 in a TV-set is as close as possible to the colour-matrix device (last part in the YUV- path).

5.2. Latchup & ESD:

ESD:

Human-body-model (100 pF, 1500 Ohm): all pins > 3000 Volts.
Machine Model (200 pF, 0 Ohm): all pins > 300 Volts.

(according to quality specification SNW-FQ-611/part E)

Latchup:

At an ambient temperature of 70° Celcius all pins meet the specification of:

$I_{trigger}$ > 100 mA or V_{pin} > 1.5 * Vcc,max
$I_{trigger}$ < -100 mA or V_{pin}< -0.5*Vcc,max

6. Advanced applications:

6.1. Y-C MODE APPLICATION

For this application, the LTP-booster is placed in front of the colour-decoder and SYNC-processor units.

As this IC has no internal timing pulses derived from the Y-signal, it depends upon the sandcastle-signal timing at pin1 of the IC.

Even though the sandcastle signal is made of the output signal of the LTP-booster, this loop-back cannot cause any clamping problems in the LTP-booster IC.

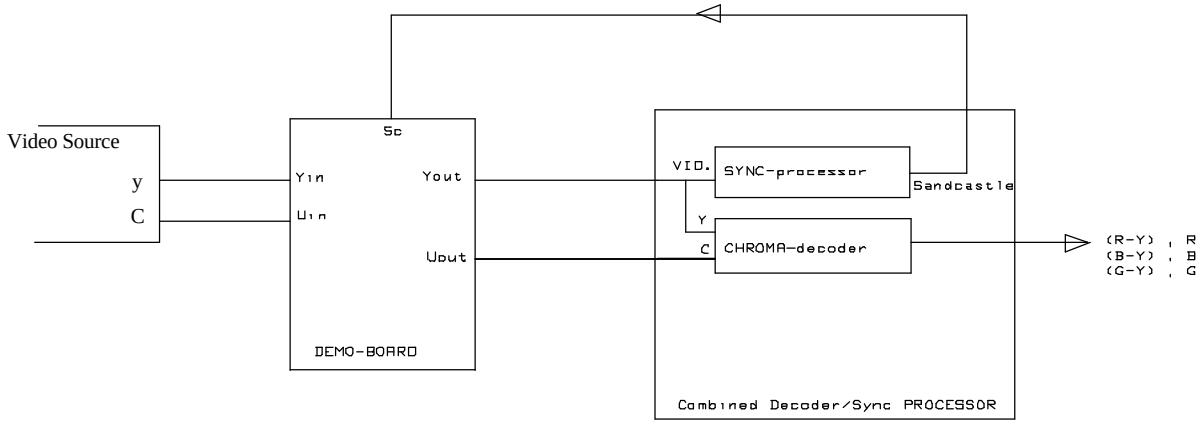


FIGURE 6.1.1.

6.1.1. Additional Application info

One of the colour-difference input's (U,V) of the LTP-booster-demo board can be used for the chroma-path (C), the other input (not used) should be connected to ground. The bandwidth of the U,V-signal amplifiers of the LTP-booster IC are large enough to allow the chroma to be processed correctly.

The DEMO-BOARD has been designed to process Y/U/V-signals. To make Y/C-mode possible, some external components are required (see FIGURE 6.1.1.1).

Make following changes external:

1. The input signals to the board must be applied through 75 Ohm resistance's, if a direct coupling to a generator is required.
2. The output signals must be buffered with emitter-followers, when driving 75 Ohm load.
3. The not used input must be shorted to ground.
4. As the Y-signal of the Y/C-bus has 1.0 Volts pp, and the TDA9177 expects 1.3 Volts pp, the Y-signal must be amplified; and the output signal must be attenuated with the same factor to make a optimum signal-performance.

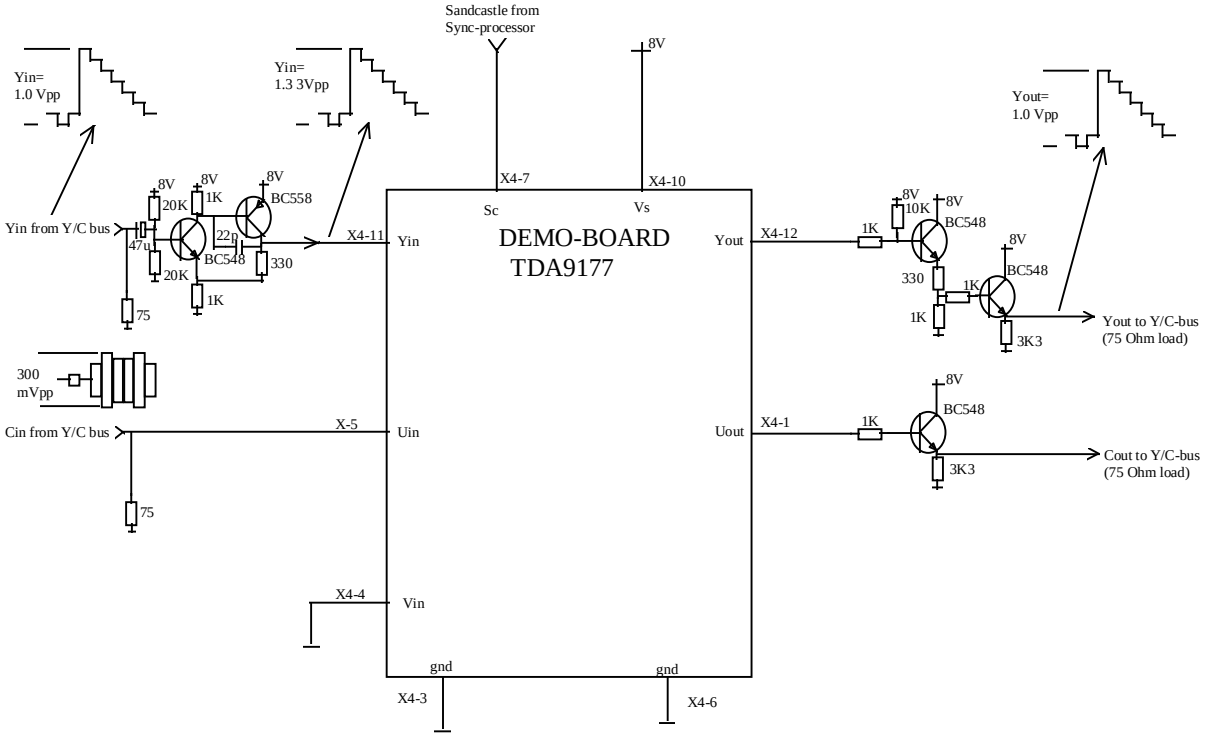

Sandcastle from
Sync-processor
8V
Yin=
1.0 Vpp
Yin=
1.3 3Vpp
Yout=
1.0 Vpp
X4-7
X4-10
Sc
Vs
DEMO-BOARD
TDA9177
Yin from Y/C bus
X4-11
Yin
Yout
X4-12
8V
20K
1K
BC558
47u
22p
BC548
330
75
10K
3K3
Yout to Y/C-bus
(75 Ohm load)
300
mVpp
Cin from Y/C bus
X-5
Uin
Uout
X4-1
Cout to Y/C-bus
(75 Ohm load)
X4-4
Vin
gnd
X4-3
X4-6

FIGURE 6.1.1.1.

6.2. Automatic Coring Control using the TDA9177

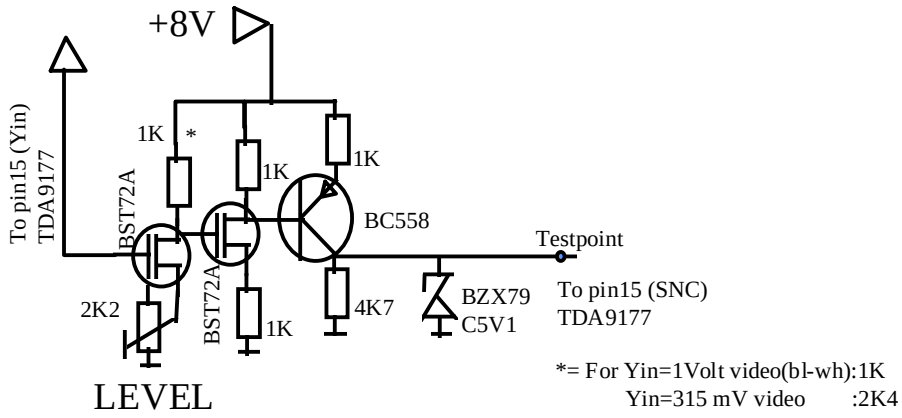
The basic idea of this note is to use the SNC-control pin of the TDA9177 to reduce the peaking effect in those parts of the picture where the scene is very dark, in order to avoid the boosting of the noise in a video signal special in the dark parts.

The SNC-control pin (pin15) is basically designed for use with the NOISE-detector of the new TDA9170A (picture-booster) IC from PHILIPS.
The CORING and STEEPNESS of the TDA9177 will be affected when the voltage of pin15 is increased. For V15=0 V, means: MINIMUM CORING and MAXIMUM STEEPNESS; for V15= Vref (about 4 Volts made by the TDA9177), means: MAXIMUM CORING and MINIMUM STEEPNESS {see appendix 1}.

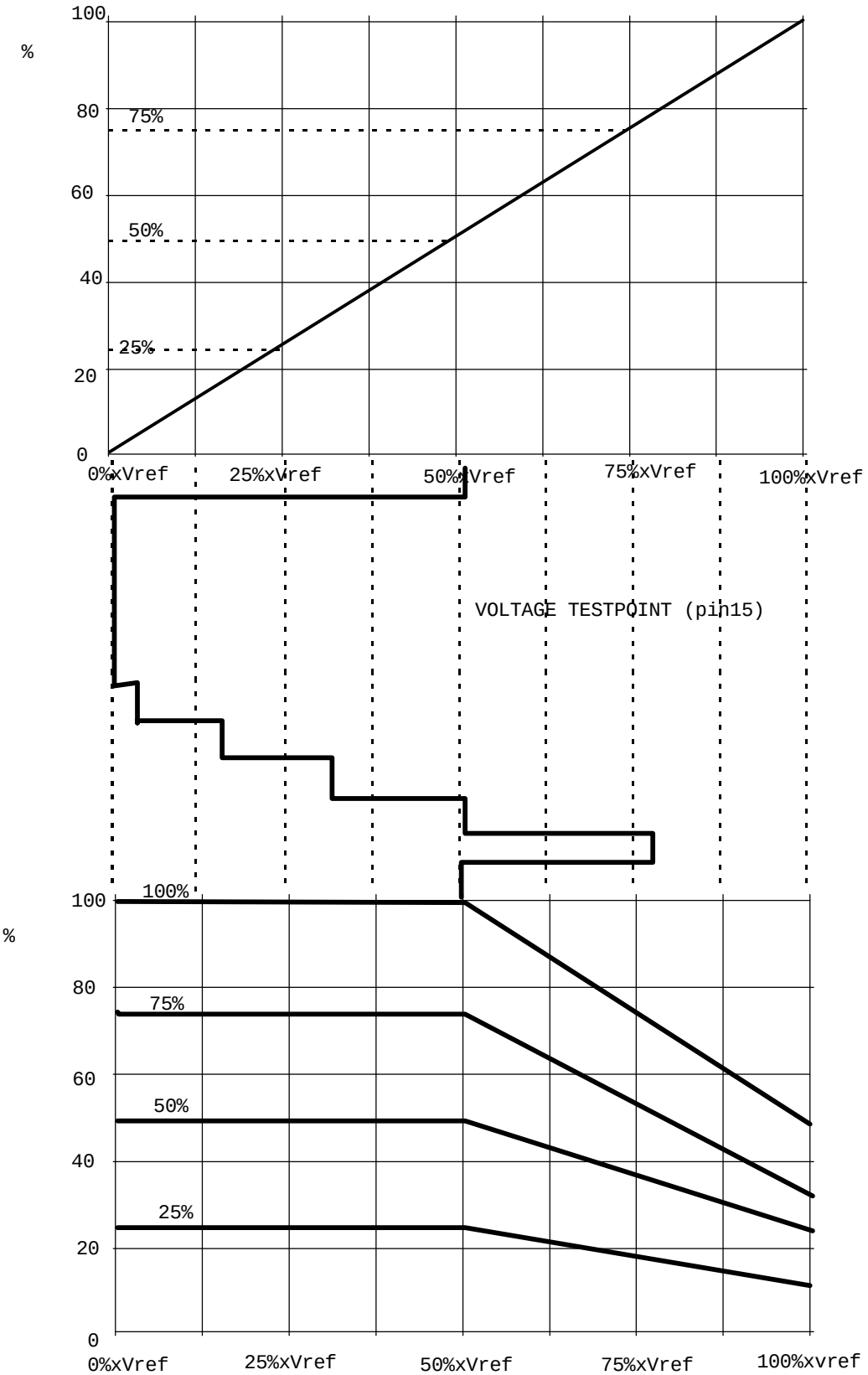
The amount of CORING (maximum setting) is determined by the voltage of pin2 (CORING-control pin), and the amount of STEEPNESS (maximum setting) is determined by the voltage of pin22 (STEEPNESS-control pin).

Now to make the CORING-control automatic, the video-signal must be amplified to fit in the range 0V till Vref/2 (about 2 Volts), and inverted so that the dark parts have high voltage at pin15 and the white parts have 0 Volts at pin15.

A very simple circuit to make this possible is given below, this circuit uses the clamp voltage of the Yinput pin of the TDA9177 for biasing, and therefore the input must be directly connected to pin5 (after the clamp capacitor); the input impedance is high enough to leave the clamping unaffected.
The zener diode (BZX79-C5V1) in this circuit is used to prevent overvoltage to pin15 (it also makes the control signal slow, this is however not so important). **For this application, remove the 100 nF capacitor which is on the demo-board at pin15.**



Relative increase of coring level as function of pin SNC, starting from different coring level presets

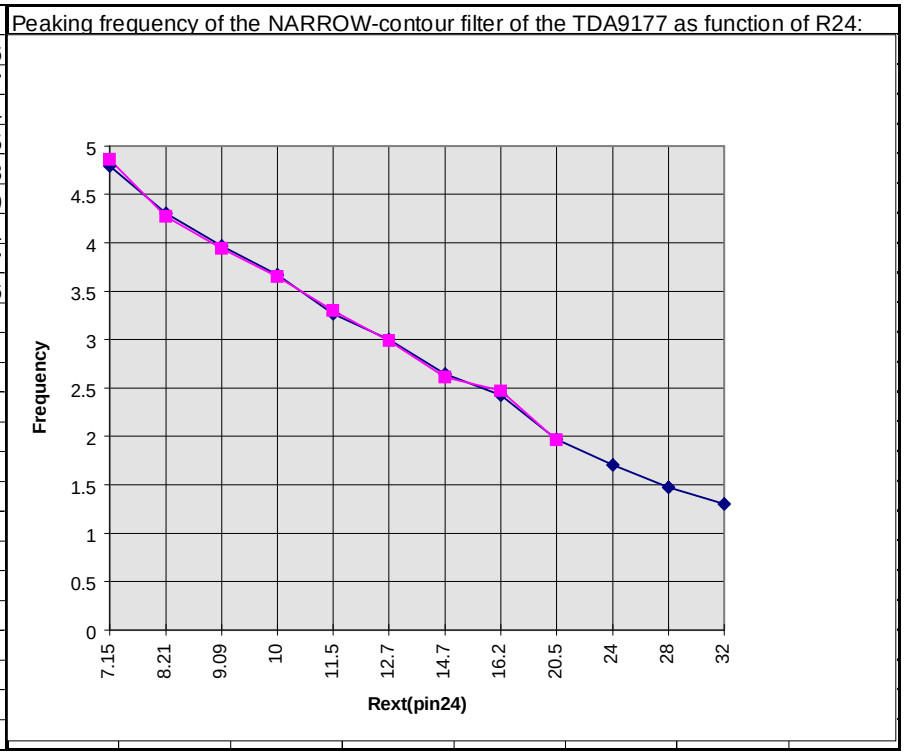


Relative decrease of steepness level as function of voltage at pin SNC, starting from four different steepness level presets

6.3. Using other Peaking frequencies:

There is a possibility of configuring the TDA9177 for other peaking frequencies by adjusting the external resistance of PIN24.
Another peaking frequency is perhaps more efficient for NTSC-signals.
Tests have revealed that just acceptable resistance values for R24 lie within 8 Kohm till 16 Kohm, and therefore the peaking frequency is limited from 4.3 MHz till 2.4 MHz.

Resistance	calculated	tested
7.15	4.7947718	4.86
8.21	4.3033204	4.27
9.09	3.9658571	3.94
10	3.6683786	3.65
11.5	3.2647198	3.3
12.7	3.0005791	2.99
14.7	2.6440407	2.61
16.2	2.4276912	2.47
20.5	1.966433	1.96
24	1.7030553	
28	1.476974	
32	1.303883	



The peaking frequency can be calculated by the formula: freq[MHz}=1/(0.02247*REXT[KOhm]+0.0479).

There are some restrictions of changing the resistance at pin24 of the TDA9177:

- The group delay time of the internal delayline will be shifted, therefore **all filters will be shifting** according to the value of the external resistance. The Narrow contour filter, the wide contour filter and the step detector will shift too.

- The delaytime per section will be shifted too, this means that **the bandwidth of the device will be shifted**, because the Tau_group*Bandwidth = constant. An increase in resistance causes a lowering of the peaking frequency, but also the bandwidth will be lower. Therefore a 'Ringing-effect' may occur when frequency components higher than the group-delay bandwidth of the device are applied. (at Rext=10 Kohm, the Tau_group-bandwidth=5.5 MHz, but when Rext=16K, the Tau_group-bandwidth is only 3.4 MHz.

- Because the **Stepdetector, to whom the activation levels are compared, is shifting too**, the relation between stepdetector and contour-filters is only optimal if Rext = 10 Kohm. For instance the 'blooming up' of the spots on the picture screen can occur because the peaking limiter is not working correct.

7. References:

- PRELIMINARY DEVICE SPECIFICATION
  Y/U/V TRANSIENT IMPROVEMENT PROCESSOR TDA9177:
  Stuivenwold & v.Dommelen
  96/02/22
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